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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,295	08/27/2003	Teiichiro Nishizaka	NEG-302US	4465

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MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,295	NISHIZAKA ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *32-38* is/are withdrawn from consideration.

5)☒ Claim(s) *21 and 24-31* is/are allowed.

6)☒ Claim(s) *1-14,22 and 23* is/are rejected.

7)☒ Claim(s) *15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the abstract exceeds 150 words. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities: in line 17 of page 11, "performing" should be deleted.

Appropriate correction is required.

Claim Objections

4. Claims 1 – 26 are objected to because of the following informalities:

in line 19 of claim 1, "other" should be replaced with "another";

in line 3 of claim 3, ":" should be replaced with ";";

in line 13 of claim 6, "ands aid" should be replaced with "and said";

in line 12 of claim 22, "other" should be replaced with "another";

in line 16 of claim 12, "other" should be replaced with "another"; and

in line 2 of claim 23, "the" should be inserted between "to" and "other".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 6 – 20, 22 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 6 recites the limitation "said layer" in line 18. There is insufficient antecedent basis for this limitation in the claim. Accordingly, it is not possible to determine the scope of the claim, since it is not known what layer the bit lines are supposed to be formed on.

Line 3 of claim 22 recites the limitation, "a plurality of sets comprising said first to fourth unit cells...". Line 6 of claim 22 recites the limitation, "a plurality of sets, each set comprising said first to fourth unit cells...". The claim language is confusing because it cannot be determined if the claim is drawn to two plurality of sets, or what it is from the first to fourth unit cells that comprise the plurality of sets being claimed. It is not clear if these "sets" are physical characteristics or a matter of selecting several physical structures that have been claimed already.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 6 – 13 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,760,437 to Shimoji.

Regarding claim 6, Shimoji teaches a semiconductor memory device (Figs. 1 and 2A) including:

a semiconductor substrate (22); and

a plurality of memory cells constituting a cell array; wherein for each adjacent two memory cells in said cell array, there are provided:

first, second and third diffusion regions (K31, K42, K53) formed in said semiconductor substrate and separated from one another;

a first insulating film (LF) formed on said semiconductor substrate and covering a region between said first diffusion region and said second diffusion region;

a first gate electrode (WL2) formed on and overlaying said first insulating film;

a second insulating film (LF) formed on said substrate and covering a region between said second diffusion region and said third diffusion

region; and

a second gate electrode (WL3) formed on and overlaying said second insulating film;

said semiconductor memory device further comprising:

first to third bit lines (BL3, BL4, BL5) provided over said semiconductor substrate and connected via associated contacts to said first, second and third diffusion regions respectively; and

first and second word lines connected respectively to said first and second gate electrodes;

wherein

a memory cell transistor including diffusion regions, said first insulating film, and said first gate electrode constitutes a first memory cell; and

another memory cell transistor including said second and third diffusion regions, said second insulating film, and said second gate electrode constitutes a second memory cell.

Regarding claim 7, Shimoji teaches a memory device, wherein each of said first and second insulating films comprises an electric charge trapping film.

Regarding claim 8, the claim only recites the preferred method of using the claimed device and has not been given patentable weight. A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

Regarding claim 9, Shimoji teaches a memory device, wherein

the second bit line is extended from one side to other side of said cell (Fig. 1). The limitation with respect to how programming is accomplished is not given any patentable weight, since this is an intended method of use limitation, as discussed above.

Regarding claims 10 and 11, limitations with respect to how programming is accomplished is not given any patentable weight, since this is an intended method of use limitation, as discussed above.

Regarding claim 12, Shimoji teaches a memory device further comprising means for determining whether said memory cell to be read is a programmed cell or an unprogrammed cell according to a magnitude of current flowing between two of the diffusion regions for said memory cell transistor (See Fig. 5, for example). The limitation with respect to how programming is accomplished is not given any patentable weight, since this is an intended method of use limitation, as discussed above.

Regarding claim 13, Shimoji teaches a memory device, wherein said first and second gate electrodes are made up of a polycrystalline silicon film, and at least one gate electrode of said first and second gate electrodes includes a metal silicide layer on a surface thereof (Col. 9, lines 28 – 31).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoji in view of Japanese Patent Publication No. 05-174583 to Masato.

Regarding claim 1, Shimoji teaches a semiconductor memory device (Fig. 22, for example) comprising:

a semiconductor substrate (22);

a plurality of unit cells constituting a cell array;

a first bit line (BL5) for read operation provided on a layer provided over the semiconductor substrate; and

a second bit line (BL4) for program and erase operations provided on the layer provided over the semiconductor substrate;

wherein said unit cell includes a memory transistor comprising:

first and second diffusion regions (S53, D53) provided in the semiconductor substrate and separated from each other;

an insulating film (LF53) including an electric charge trapping film, formed on the semiconductor substrate and covering a region between said first and second diffusion regions; and

a gate electrode (WL3) formed on and overlaying said insulating film to constitute a word line electrode; and wherein

at least one of said first diffusion region and said second diffusion region (S53) in said each unit cell is shared by another unit cell adjacent to said unit cell; and

said first and second diffusion regions are connected to said first and second bit lines respectively.

Shimoji does not teach a memory device in which each four unit cells share a contact region and are arranged in an X pattern with said contact region being a center thereof. Masato teaches a memory device in which each four unit cells share a contact region and are arranged in an X pattern with said contact region being a center thereof (See Abstract and Figs. 1 – 6). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Masato into the device taught by Shimoji, since it is desirable to reduce the occupying area of a memory cell.

Regarding claim 2, the claim only recites the preferred method of using the claimed device and has not been given patentable weight. A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

Regarding claim 3, Shimoji teaches a memory device, wherein the insulating film comprises:

a silicon dioxide film formed on the semiconductor substrate;

a silicon nitride film formed on and overlaying the silicon dioxide film; and

a silicon dioxide film formed on and overlaying the silicon nitride film (Col. 9, lines 14 – 20).

Regarding claim 4, Shimoji teaches a memory device, wherein surface of the gate electrode comprises a metal silicide (Col. 9, lines 28 – 31).

Regarding claim 5, Shimoji teaches a memory device, wherein the second bit line is extended from one side to the other side of the cell array (Fig. 1). The limitation with respect to how programming is accomplished is not given any patentable weight, since this is an intended method of use limitation, as discussed above.

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoji as applied to claims 6 and 13 above, and further in view of US Patent No. 5,751,631 to Liu et al.

Shimoji does not teach a memory device, wherein first to third diffusion regions include metal silicide. Liu et al. teach a memory device, wherein metal silicide is formed on the diffusion regions (Fig. 3F). It would have been obvious to one of ordinary skill in the art incorporate the teaching of Liu et al. into the device taught by Shimoji, since it is desirable to provide low resistance contacts.

Allowable Subject Matter

13. Claims 15 – 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 21 and 24 – 31 are allowed.

15. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach, alone or in combination, a memory device including, "a first word line connected in common to said first gate electrode and said second gate electrode", "a second word line connected in common to said third gate electrode and said fourth gate electrode" and "a first bit line...crossing over said

first and second word lines" and second and third bit lines crossing over first and second word lines. The prior art does not teach a method of controlling a semiconductor memory device including "setting the other bit line to a third positive program inhibiting voltage".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DWO

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800